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09/638,245	08/14/2000	Christopher M. Hanna	56233-139(THAT-3DVCN0	1379

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EXAMINER	
LEE, PING	

ART UNIT	PAPER NUMBER
2614	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mweipdocket@mwe.com

Office Action Summary	Application No.	Applicant(s)	
	09/638,245	HANNA, CHRISTOPHER M.	
	Examiner	Art Unit	
	Ping Lee	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *60-93,106,109,112-115,117 and 119* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *60-93,106,109,112-115,117 and 119* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In view of pre-appeal request filed on 10/4/10, Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, "the difference between the summation signal and the difference signal, for a given frequency and level, conforms with the difference specified by the BTSC standard" as specified in claims 69, 78, 80, 82, 86 and 110 and a similar language in claims 112-114; "the BTSC encoder has a frequency response in the digital domain that is substantially equal to the analog frequency response specified by the BTSC standard" as specified in claim 87; "the digital matrix has a frequency response in the digital domain that is substantially equal to the analog frequency response specified by the BTSC standard" as specified in claim 89 and the similar language in claim 92; "the digital signal processor has a frequency response in the digital domain that is substantially equal to the analog frequency response specified by the BTSC standard" as specified in claim 109 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate

prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 87 and 115 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 87, from line 3, the digital composite modulator has been specified to include a difference channel processing section and a sum channel processing section. This is not a correct description. It is the encoder that includes a different channel processing section and a sum channel processing section.

Claim Rejections - 35 USC § 103

5. Claims 69-71, 78-87, 89-93, 106, 109, 110, 115, 117 and 119 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gibson et al. (hereafter Gibson; US 4,760,602) in view of the prior art as shown in Fig. 1 (hereafter AAPA).

Regarding claim 86, Gibson discloses a BTSC processor for L-R signal at the transmitter (shown in Fig. 1A; col. 2, lines 56-60; col. 1, lines 5-24)) and a BTSC processor at the receiver (shown in Fig. 1B). The adaptive weighting circuit could be implemented in analog or digital form (col. 8, lines 11-16). Thus, Gibson meets the claimed limitation as specified in B.

Gibson fails to show the processor for L+R signal at the transmitter. However, BTSC encoder at the transmitter inherently includes processor for processing L+R signal. AAPA clearly illustrates a processor for processing L+R signal and another processor for processing L-R signal. As illustrated in AAPA, the processor for processing L+R signal is simpler than the processor for processing L-R signal. By using digital circuit for implementing a digital processor for processing L-R signal as suggested in Gibson, one skilled in the art could expect that a digital processor could be designed for processing L+R signal without undue experience.

Gibson teaches that L-R signal is in a general sampled data form (col. 8, line 13). Nevertheless, Gibson fails to explicitly teach how to do so. Thus, one skilled in the art would have expected that any well known method for converting and sampling the left

and right signals could be used. The sampled left and right signals would form the digital L+R signal and the digital L-R signal.

The limitation as defined in D is inherently met according to BTSC standard that complies by Gibson and AAPA.

Thus, it would have been obvious to one of ordinary skill in the art to combine Gibson and AAPA by designing a digital processor for L+R signal and a digital processor for L-R in order to process both the L+R signal and the L-R in digitized form.

Regarding claims 87 and 115, the claimed system, comparing with claim 86, further includes a digital composite modulator. Gibson teaches a modulator (col. 2, line 65+). As discussed in claim 86, the L+R signal and the L-R signal are digitally processed. L+R signal or the L-R signal is a digital composite signal. So the modulator used for modulating the digital L+R signal and the digital L-R signal could read on the claimed digital composite modulator. The limitation that the BTSC encoder has a frequency response in the digital domain that is substantially equal to the analog frequency response specified by the BTSC standard is an inherent feature when one skilled in the art designs the digital processor for processing L+R signal and the digital processor for processing L-R signal as specified as the BTSC encoder.

Claim 89 is similar to claim 86.

Regarding claim 90, Gibson and AAPA fail to show that the digital matrix unit, the difference channel processing unit, and the sum channel processing unit are included in a single integrated circuit. When an engineer designs a system, the size of the system is a very important factor to be considered due to the cost of manufacturing, shipping,

weight, and overall appearance of the product. With the advanced technology, the size of an electronic circuit, in general, has reduced dramatically. Thus, it would have been obvious to one of ordinary skill in the art to modify the combination of Gibson and AAPA to try to placing the digital matrix unit, the difference channel processing unit, and the sum channel processing unit in a single integrated circuit in order to reduce the cost of the system and make a smaller system.

Regarding claim 91, Gibson and AAPA fail to show that the digital matrix unit, the difference channel processing unit, and the sum channel processing unit are implemented by a DSP. Gibson suggests a general digital circuitry. Examiner takes Official Notice that using a DSP to perform the digital processing function is notoriously well known in the art. Thus, it would have been obvious to one of ordinary skill in the art to further modify Gibson and AAPA by using well known DSP in order to program the DSP to perform the digitized encoding function.

Regarding claims 69, 70, 78, 79, 80, 81, Gibson further fails to show a digital-to-analog converter arrangement. By digitally processing the L+R signal and the L-R signal, they are digitally encoded signals. Gibson teaches a general modulator (col. 2, lines 65+). A general analog modulator or a general digital modulator is well known in the art. With a general analog modulator, the digitally processed L+R signal and the digitally processed L-R signal have to be converted to analog format in order to be transmitted by the analog modulator. That is, DACs are at the inputs of a general analog modulator. On the other hand, when using a digital modulator, a DAC, at the output of the digital modulator, could be used to convert the modulated digital signal to

analog signal. Examiner takes Official Notice that DAC is notoriously well known in the art. Thus, it would have been obvious to one of ordinary skill in the art to further modify Gibson and AAPA by including well-known DAC in order to use the analog modulator to combine the digitally processed L+R signal and L-R signal, or using well-known DAC for converting the digitally modulated composite signal.

Regarding claims 71, the claimed "preselected sample rate" is inherently included in a digital signal.

Regarding claims 82, 83 and 85, the limitation specified in this claims has been discussed in claim 86 above.

Regarding claim 84, the claimed 75 μs preemphasis is inherently included according to BTSC standard.

Regarding claim 92, comparing with claim 87 discussed above, Gibson fails to show that the matrix unit has a frequency response in the digital domain that is substantially equal to the analog frequency response specified by the BTSC standard. The function of the matrix unit is to generate a L+R signal and a L-R signal. The AAPA discloses a matrix unit. This matrix unit could be easily designed to generate a digital L+R signal and a digital L-R signal without undue experience. The frequency response of the digital matrix unit should be similar to the frequency response of the equivalent analog matrix unit in order to preserve the signal contents (sum and difference signals). Examiner takes Official Notice that this feature is notoriously well known in the art. By using such matrix unit, the digital L-R signal could be processed by the digital

processing unit as suggested in Gibson. Using a digital matrix has been discussed in claim 86 above.

Regarding claim 93, the claimed frequency is an inherent feature of a BTSC broadcasting signal.

Regarding claims 106 and 117, the limitations in the claims are similar to those in claims 86 and 87 with the exception of the adaptive signal weighting system configured to dynamically vary the phase of the digital difference signal, and the digital sum channel section comprising one or more digital filters for altering the phase of the digital sum signal. Gibson hints that the adaptive network for processing the difference signal would inherently vary the phase (col. 2, lines 12-18). Gibson also teaches that matching delays and synchronizing latches may be required between particular circuit elements which would be known to those in the art (col. 8, lines 17-19). Although Gibson's suggestion is not directly toward the digital sum channel section, Gibson's suggestion applies to all circuit sections that require synchronization. The stereophonic signal to be broadcasted using BTSC encoder requires synchronization between the processed L+R signal and the processed L-R signal. Thus, it would have been obvious to one of ordinary skill in the art to further modify the combination of Gibson and AAPA by including necessary delays in the digital sum channel section in order to provide synchronized L-R signal and the L+R signal to the modulator.

Regarding claims 109 and 119, the limitations in the claims are similar to those in claims 86 and 87 with the exception of the digital signal processor has a frequency response in the digital domain that is substantially equal to the analog frequency

response specified by the BTSC standard. As discussed above, Gibson suggests that the variable preemphasis network, which processes the L-R signal, could be implemented in either analog or digital form. Gibson does not emphasis whether one should use a digital variable preemphasis network or the analog one. Thus, one skilled in the art would have reasonably concluded that they are functionally equivalent, hence, they produce similar result. The frequency response of the digital variable preemphasis network would have been substantially equal to the analog preemphasis network.

The circuit for processing L+R signal is simple and straight forward comparing with the circuit for processing L-R signal (see Fig. 1 of AAPA; this has been discussed for claim 86 above). When Gibson suggests digital variable preemphasis network, one could design and implement in digital circuit for processing L+R signal as well without undue experience. As with the digital for processing the L-R signal, one skilled in the art would have reasonably concluded that the digital circuit for processing L-R signal should be functionally equivalent to the analog circuit, hence, they produce similar result. The frequency response of the digital circuit for L+R would have been substantially equal to the analog circuit for L+R.

The same logic applied to the combining section as well.

Claim 110 is similar to claim 109.

6. Claims 60-68, 72-77, 88 and 112-114 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gibson and AAPA as applied to claims 69-71, 78-87, 89-93,

106, 109, 110, 115, 117 and 119 above, and further in view of Crochiere et al. (hereafter Crochiere) ("Interpolation and Decimation of Digital Signals - A Tutorial Review").

Regarding claims 88, 72-77, Gibson and AAPA fail to show a first up-sampler configured to insert additional samples into the summations signal to increase the sample rate of the summation signal and a second up-sampler configured to insert additional samples into the difference signal to increase the sample rate of the difference signal. Crochiere teaches sampling general digital signals. According to Crochiere, the sampling rate is a fundamental consideration of digital signal processing techniques and applications. It determines the convenience, efficiency, and/or accuracy in which the digital signal processing can be performed. The sampling rate can be and should be converted to a different one so the resulting signal corresponding to the same analog function or to convert rate in the system from one rate to another when performing different parts of processing algorithm at different sampling rates (second column of p. 300 and abstract). When the rate needs to increase, Crochiere teaches using interpolation. When the rate needs to decrease, Crochiere teaches using decimation. The analog circuit as shown in AAPA involves many signal processing steps. Specifically, the sum signal and the difference signal are processed separately and fundamentally differently. Thus, with Gibson, AAPA and Crochiere in front of him/her, it would have been obvious to one of ordinary skill in the art to combine them to form a digital BTSC encoder with necessary interpolator and/or decimator in order to ensure that the digital BTSC encoder would generate a signal that corresponds to the

analog signal according to the analog BTSC encoder and the digital BTSC encoder would produce signal with accurate data with great efficiency.

The claimed 75 μs preemphasis is inherently included according to BTSC standard. The claimed "digital signal processor" could also be interpreted as a circuit for processing digital signal.

Regarding claims 60, 61, 63-65, 67, 68, Gibson further fails to show a digital-to-analog converter arrangement. By digitally processing the L+R signal and the L-R signal, they are digitally encoded signals. Gibson teaches a general modulator (col. 2, lines 65+). A general analog modulator or a general digital modulator is well known in the art. With a general analog modulator, the digitally processed L+R signal and the digitally processed L-R signal have to be converted to analog format in order to be transmitted by the analog modulator. That is, DACs are at the inputs of a general analog modulator. On the other hand, when using a digital modulator, a DAC, at the output of the digital modulator, could be used to convert the modulated digital signal to analog signal. Examiner takes Official Notice that DAC is notoriously well known in the art. Thus, it would have been obvious to one of ordinary skill in the art to further modify Gibson and AAPA by including well-known DAC in order to use the analog modulator to combine the digitally processed L+R signal and L-R signal, or using well-known DAC for converting the digitally modulated composite signal.

Regarding claims 62, 66 and 75, the claimed "preselected sample rate" is inherently included in a digital signal.

Regarding claims 112-114, the signal transformation arrangement reads on the up sampler which has been discussed with respect to claim 88 above.

Response to Arguments

7. Applicant's arguments with respect to claims 60-93, 106, 109, 110, 112-115, 117 and 119 have been considered but are moot in view of the new ground(s) of rejection.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ping Lee whose telephone number is 571-272-7522. The examiner can normally be reached on Wednesday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivian C. Chin can be reached on 571-272-7848. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ping Lee/
Primary Examiner, Art Unit 2614

pwl